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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/045,913
Filing Date: January 09, 2002
Appellant(s): SINGH ET AL.

Joanna G. Chiu
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/28/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that Group A claims (i.e., claims 1-10 and 15-28) and Group B claims (i.e., claims 29-34 and 38-42) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,245,641	Shiozawa et al.	6-2001
5,994,201	Lee	11-1999
5,578,518	Koike	11-1996

S. Wolf (Silicon Processing for VLSI Era, volume 1, pages 532-533, 1986).

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

a. Claims 1-2, 5, 8-10,15, 19 and 23-27, 29 and 32-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiozawa et al., US patent No. 6,245,641.

Regarding claims 1 and 15, Shiozawa teaches (figs. 2-9) a method for forming a semiconductor device structure in a semiconductor layer, comprising: forming a first trench of a first width (4b, 4c) and a second trench of a second width (4a) in the semiconductor layer; forming a first insulator liner (5b, 5c and 8) in the first trench and a second insulator liner (5a and 8) in the second trench; forming a mask (12) over the second trench; etching at least a portion of the first insulator liner while the mask is over the second trench; removing the mask; and depositing an insulating layer (6) in the first trench and the second trench.

Shiozawa teaches more than one layer of oxide liner.

Regarding claim 2, Shiozawa teaches (fig. 3) the entire claimed process of claim 1 above including the first width (4b, 4c) is less than the second width (4a).

Regarding claim 5, Shiozawa teaches (figs. 4 and 5) the entire claimed process of claim 1 above including the step of forming the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

Regarding claim 8, Shiozawa teaches (fig. 8, col. 10, line 36-44) the entire claimed process of claim 1 above including the insulator layer comprises high-density plasma oxide fill.

Regarding claim 9, Shiozawa teaches (fig. 3) the entire claimed process of claim 1 above including forming a barrier layer (3a-3d) and a stress relief layer (2a-2d) over the semiconductor layer in areas adjacent to the first trench and the second trench.

Regarding claim 10, Shiozawa teaches (figs. 2 and 3) the entire claimed process of claim 1 above including a pad nitride (3a-3d) and pad oxide (2a-2d) over the semiconductor layer prior to forming the first trench and the second trench, and wherein the step of forming the first trench and the second trench comprises etching through selected portions of the pad nitride and the pad oxide and into the semiconductor layer.

Regarding claims 19 and 23-25, Shiozawa teaches (figs. 2, 3 and 7) the entire claimed process of claim 1 above including the step of forming the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

Regarding claims 26, 27 and 29, Shiozawa teaches (figs. 3, 7 and 8) the entire claimed process of claim 1 above including the step of forming the first insulator liner comprises growing oxide at a high temperature (figure 8 shows portion of the second insulator liner etched).

Shiozawa teaches forming thermal oxidation process for forming liners 5a to 5c (col. 9, line 14-30). This process inherently involves high temperature process.

Regarding claim 32, Shiozawa teaches the entire claimed process of claim 29 above including the first insulator liner (5b, 5c and 8) and the second insulator liner (5a and 8) comprises thermal oxide (col. 10, line 1-4).

Regarding claim 33, Shiozawa teaches the entire claimed process of claim 29 above including the step of depositing comprises filling the first trench and second trench (fig. 9).

Regarding claim 34, Shiozawa teaches (fig. 8, col. 10, line 36-44) the entire claimed process of claim 29 above including the insulating layer (6) comprises high-density plasma oxide (fig. 8).

b. Claims 3, 4, 6, 16, 17, 18, 22, 28, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa et al.

Regarding claim 3, Shiozawa teaches (fig. 7) the entire claimed process of claim 1 above except explicitly stating that the step of etching comprises completely removing the first insulator liner.

It is conventional in the art to completely remove oxide liners in a trench after forming them.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to completely remove the first liner oxide taught by Shiozawa since oxide liners are some times formed to minimize the damage done during etching process and removed afterwards.

Regarding claims 4, 22, 28, 40 and 42 Shiozawa teaches substantially the entire claimed process of claims 1, 15, 26 and 38 above except explicitly stating that the step of etching results in leaving at least one hundred, fifty angstroms of the first and fifty angstroms of the second insulator liner.

Parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the thickness of the oxide liner in the process of Shiozawa as claimed in order to form a trench isolation.

c. Claims 6, 16, 17, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view S. Wolf (Silicon Processing for The VLSI Era, volume 1, pages 532-533).

Regarding claims 6, 16, 17, 30, 31 Shiozawa teaches substantially the entire claimed process of claims 1,15 and 29 above except explicitly stating that the step of etching comprises a wet etch where the process comprises dipping the semiconductor device structure in hydrofluoric acid.

It is conventional and also taught by Shiozawa using wet etch process for removing portion of the oxide layer (8) in figure 12. Also hydrofluoric acid is a conventionally used etchant of oxide layer and is also taught by Wolf (starting paragraph 4 page 532).

It would have been obvious to one of ordinary skill in the art at the time the invention was made in corporate the conventional HF etchant Taught by Wolf in the process of Shiozawa because HF etches silicon oxide quickly for good process control.

Regarding claims 7 and 18, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above except explicitly stating that the step of etching comprises applying etch chemistry to the semiconductor device.

The use of dry etching for removing oxide layer is a conventional process that is widely known and also taught by Lee (fig. 2E) for removing oxide layer (206).

It would have been obvious to one of ordinary skill in the art at the time the invention was made in corporate the conventional process of using dry etching process taught by Lee in the process of Shiozawa in order to uniformly etch the oxide liner.

Regarding claim 20, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above including the semiconductor layer has a top surface; the second trench has a corner where the trench adjoins the top surface of the semiconductor layer.

Shiozawa does not teach the step of forming the first insulator liner and the second insulator liner comprising rounding of the corner of the second.

Lee teaches (fig. 2c) forming liner (214) in such a way the corners in the trenches (210) and (212) are rounded.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include forming rounded corners as suggested by Lee in the

process steps of Shiozawa in order to avoid kink effects that decrease the threshold voltage of the device (col. 2. line 9-20).

Regarding claim 21, Shiozawa teaches substantially the entire claimed process of claim 20 above including the corner is a semiconductor (fig. 2c).

d. Regarding claims 38-41, Shiozawa teaches substantially the entire claimed process of claims 20, 29, 32, 33 and 34 above including etching a portion of the second insulator liner (portion of 8a is removed figure 8).

Shiozawa does not teach growing a first insulator liner in the first trench and a second insulator liner in the second trench to achieve a radius of curvature of at least 200 Angstroms in the first and second corner.

Koike teaches (see abstract) rounding of isolation trenches to achieve a radius of curvature of not less than 500 angstroms. Furthermore parameters such as radius of curvature in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the radius of curvature of corners of the first and second trenches in the process of Shiozawa as taught by Koike since rounding of the edges prevents the concentration of electric field in the edge portion of the trench isolation resulting in the prevention of the lowering of the threshold voltage (col. 2, lines 43-47, Koike).

(11) Response to Argument

Appellant's argument filed on May 3, 2004 have been fully considered but they are not persuasive.

Appellant's argued that growing is not the same as depositing an oxide layer. Furthermore applicant's argued that they chose their words deliberately to distinguish growing from depositing.

Merriam-Webster's Collegiate Dictionary (2001), Tenth Edition, defines "grow" as "to increase in size by assimilation of material into the living organism or by accretion of material in a non-biological process". Since deposition process results in accretion of material, the two processes are the same. During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir.1989).

Since the specification does not explicitly distinguish the process of growing to be any different than deposition, the reference meets the plain meaning definition of growing. Applicant does not specifically associate growing to any particular process. Without a specific process, growing is taken to mean the same or at least equivalent to as depositing. Office personal are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

SAG
July 14, 2004

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